MT6358 PMIC Technical Brief

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Document Revision History

Revision	Date	Author	Description
0.1	2017-08-14	Nick Tang	Initial draft

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.6V ~ 5V
- 9 buck converters and 33 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K-Crystal-less RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- SPI interface
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- Storage card plug-out protection
- 194-pin MIFO WLCSP package

1.2 Applications

MT6358 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6358 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 9 buck converters and 33 LDOs optimized for specific 2G/3G/4G smart phone subsystems.
Sophisticated controls are available for power-up and the RTC alarm. MT6358 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6358 adopts SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with baseband.

MT6358 is available in a 194-pin MIFO WLCSP package. The operating temperature ranges from -30 to +85°C.

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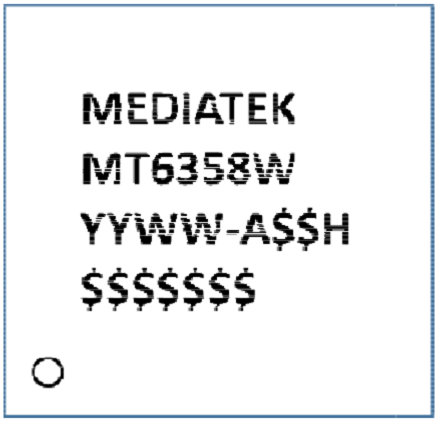
1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6358W/A		-30 ~ +85°C	FOCSP 194L

1.5 Top Marking Definition

MT6358W/A



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1.6 Pin Assignments and Descriptions

194	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	VS1	GND_VS1	VPA	VSYS_VPA	VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	NC	A
B	VSYS_VS1	VS1	GND_VS1	GND_VPA		VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	GND_VCORE_FB	B
C	VSYS_VS1														GND_VGPU_FB	VCORE_FB	C
D		PWRKEY	EXT_PMIC_EN1	RESETB	VPA_FB	VPROC11_FB	GND_VPROC11_FB	GND_VPROC12	GND_VPROC12	GND_VPROC12_FB	VDRAM1_FB	GND_VGPU	GND_VGPU	VGPU_FB	VMODEM_FB	VS2_FB	D
E	GND_SMPS	VSYS_SMPS	VEFUSE	VS1_LDO1	EXT_PMIC_EN2	VCAMIO	VS1_FB	PMU_TESTMODE	VPROC12_FB			GND_VDRAM1_FB		GND_VMODEM_FB			E
F	AU_V18N	FLYN	VIO18		VRF18	VCN18	D_GND	D_GND	D_GND	RTC32K_1V8_0	SPI_CLK	WDTRSTB_IN	SPI_CSN	VSYS_VMODEM	VMODEM	VMODEM	F
G		FLYP		AU_HPR	AU_LOLP	AU_LOLN	D_GND	D_GND	D_GND	SPI_MISO	SPI_MOSI	RTC32K_1V8_1	HOMEKEY		GND_VMODEM	GND_VMODEM	G
H	AVSS18_AUD	AVDD18_AUD		AU_HPL	AU_REFN	AU_HSN	D_GND	D_GND	D_GND	AUD_CLK_MISO	AUD_DAT_MISO1		SCP_VREQ_VAO		GND_VDRAM1		H
J			AVDD28_AUD	HP_EINT	AVSS28_AUD	AU_HSP	SRCLKEN_IN1	DVDD18_DIG	AUD_DAT_MOSI0	AUD_SYNC_MISO	AUD_DAT_MISO0		SD_CARD_DET_N		VDRAM1	VSYS_VDRAM1	J
K	AU_VIN0_P		AU_VIN2_N	AU_VIN2_P	AU_MICBIAS0	ACCDET				AUD_SYNC_MOSI		VCDT	CHRLDO		VSYS_VS2	VSYS_VS2	K
L	AU_VIN0_N		AU_VIN1_N	AU_VIN1_P	AU_MICBIAS1	FSOURCE	SRCLKEN_IN0	DVSS18_IO	DVDD18_IO	AUD_DAT_MOSI1	AUD_CLK_MOSI	BATON	BATADC	GND_VS2	VS2	VS2	L
M		AUXADC_VIN	AVDD18_AUXADC	AVSS18_AUXADC	CS_N	VAUX18	RTC32K_2V8	VRTC28	VBIF28	VCAMA1	VSYSSNS	VREF	UVLO_VTH	VS2_LDO4	VCAMD		M
N	XTAL1	AVSS22_XO_ISO		XO_NFC		CS_P	VSIM1	VUSB	VIO28	VCAMA2	VSYS_LDO3	VCN33	GND_VREF	VS2_LDO2	VRF12	VA12	N
P	XTAL2	AVSS22_XO	XO_WCN	XO_SOC	XO_EXT	VXO22	VSYS_LDO1	VLDO28	VSYS_LDO2	VSIM2	VIBR	VSRAM_PROC11	VS2_LDO3	VSRAM_OTHERS	VDRAM2	VRF12_S	P
R	NC	AVSS22_XOBUF	XO_CEL		VAUD28	VCN28	VFE28		VMC	VMCH	VEMC		VSRAM_PROC12	VSRAM_GPU	VS2_LDO1	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 1-1. MT6358 VFBGA 194 (6.4x6 mm) pin assignment (top view)

Table 1-1. MT6358 pin descriptions

Ball	Symbol	I/O	Description
P1	XTAL2	I/O	XTAL input 2
N1	XTAL1	I/O	XTAL input 1
P3	XO_WCN	O	26MHz output to Conn. RF
P4	XO_SOC	O	26MHz output to SOC
N4	XO_NFC	O	26MHz output to NFC
P5	XO_EXT	O	26MHz output to UFS
R3	XO_CEL	O	26MHz output to Cell. RF

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Ball	Symbol	I/O	Description
F12	WDTRSTB_IN	I	Watchdog reset from AP
P6	VXO22	O	VXO22 output voltage
N8	VUSB	O	VUSB output voltage
M11	VSYSSNS	I	VSYS supply input for internal block and UVLO detection
K15, K16	VSYS_VS2	PWR	Power supply of VS2
B1, C1	VSYS_VS1	PWR	Power supply of VS1
A10, B10	VSYS_VPROC12	PWR	Power supply of VPROC12
A6, B6	VSYS_VPROC11	PWR	Power supply of VPROC11
A5	VSYS_VPA	PWR	Power supply of VPA
F14	VSYS_VMODEM	PWR	Power supply of VMODEM
A11, B11	VSYS_VGPU	PWR	Power supply of VGPU
J16	VSYS_VDRAM1	PWR	Power supply of VDRAM1
A15, B15	VSYS_VCORE	PWR	Power supply of VCORE
E2	VSYS_SMPS	PWR	Power supply of buck controller
N11	VSYS_LDO3	PWR	Power supply input of LDO group 3
P9	VSYS_LDO2	PWR	Power supply input of LDO group 2
P7	VSYS_LDO1	PWR	Power supply input of LDO group 1
R13	VSRAM_PROC12	O	VSRAM_PROC12 output voltage
P12	VSRAM_PROC11	O	VSRAM_PROC11 output voltage
P14	VSRAM_OTHERS	O	VSRAM_OTHERS output voltage
R14	VSRAM_GPU	O	VSRAM_GPU output voltage
P10	VSIM2	O	VSIM2 output voltage
N7	VSIM1	O	VSIM1 output voltage
M14	VS2_LDO4	PWR	1.125VPower supply of SLDO4
P13	VS2_LDO3	PWR	1.35V Power supply of SLDO3
N14	VS2_LDO2	PWR	1.35V Power supply of SLDO2
R15	VS2_LDO1	PWR	1.125V Power supply of SLDO1
D16	VS2_FB	I	BUCK VS2 feedback pin
L15, L16	VS2	O	SW node of VS2
E4	VS1_LDO1	PWR	2V power supply of SLDO1
E7	VS1_FB	I	BUCK VS1 feedback pin

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Ball	Symbol	I/O	Description
A2, B2	VS1	O	SW node of VS1
M8	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
F5	VRF18	O	VRF18 output voltage
P16	VRF12_S	I	LDO VRF12_S feedback pin
N15	VRF12	O	VRF12 output voltage
M12	VREF	O	Bandgap reference voltage
E9	VPROC12_FB	I	BUCK VPROC12 feedback pin on Vout
A9, B9	VPROC12	O	SW node of VPROC12
D6	VPROC11_FB	I	BUCK VPROC11 feedback pin on Vout
A7, B7	VPROC11	O	SW node of VPROC11
D5	VPA_FB	I	BUCK VPA feedback pin on Vout
A4	VPA	O	SW node of VPA
D15	VMODEM_FB	I	BUCK VMODEM feedback pin on Vout
F15, F16	VMODEM	O	SW node of VMODEM
R10	VMCH	O	VMCH output voltage
R9	VMC	O	VMC output voltage
P8	VLDO28	O	VLDO28 output voltage
N9	VIO28	O	VIO28 output voltage
F3	VIO18	O	VIO18 output voltage
P11	VIBR	O	VIBR output voltage
D14	VGPU_FB	I	BUCK VGPU feedback pin on Vout
A12, B12	VGPU	O	SW node of VGPU
R7	VFE28	O	VFE28 output voltage
R11	VEMC	O	VEMC33 output voltage
E3	VEFUSE	O	VEFUSE output voltage
P15	VDRAM2	O	VDRAM2 output voltage
D11	VDRAM1_FB	I	BUCK VDRAM1 feedback pin on Vout
J15	VDRAM1	O	SW node of VDRAM1
C16	VCORE_FB	I	BUCK VCORE feedback pin on Vout
A14, B14	VCORE	O	SW node of VCORE

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Ball	Symbol	I/O	Description
N12	VCN33	O	VCN33 output voltage
R6	VCN28	O	VCN28 output voltage
F6	VCN18	O	VCN18 output voltage
K12	VCDT	I	Fractional charger input voltage for charger detection
E6	VCAMIO	O	VCAMIO output voltage
M15	VCAMD	O	VCAMD output voltage
N10	VCAMA2	O	VCAMA2 output voltage
M10	VCAMA1	O	VCAMA1 output voltage
M9	VBIF28	O	VBIF28 output voltage
M6	VAUX18	O	VAUX18 output voltage
R5	VAUD28	O	VAUD28 output voltage
N16	VA12	O	VA12 output voltage
M13	UVLO_VTH	I	UVLO threshold control pin
J7	SRCLKEN_IN1	I	Source clock enable pin 1
L7	SRCLKEN_IN0	I	Source clock enable pin 0
G11	SPI_MOSI	I/O	SPI control interface
G10	SPI_MISO	I/O	SPI control interface
F13	SPI_CSN	I/O	SPI control interface
F11	SPI_CLK	I	SPI control interface
J13	SD_CARD_DET_N	I	Voltage source request input pin, connected to SD CARD
H13	SCP_VREQ_VAO	I	Voltage source request input pin, connected to SOC
M7	RTC32K_2V8	O	VRTC domain 32kHz clock output
G12	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
F10	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
D4	RESETB	O	System reset release signal
D2	PWRKEY	I	PWRKEY button
E8	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
A1, A16, R1, R16	NC	NC	NC
J4	HP_EINT	I	HPL detection
G13	HOMEKEY	I	HOMEKEY button
L14	GND_VS2	GND	VS2 ground

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Ball	Symbol	I/O	Description
A3, B3	GND_VS1	GND	VS1 ground
N13	GND_VREF	GND	Ground for bandgap
D10	GND_VPROC12_FB	I	Remote sense on ground of VPROC12 Vout
D8, D9	GND_VPROC12	GND	VPROC12 ground
D7	GND_VPROC11_FB	I	Remote sense on ground of VPROC11 Vout
A8, B8	GND_VPROC11	GND	VPROC11 ground
B4	GND_VPA	GND	VPA ground
E14	GND_VMODEM_FB	I	Remote sense on ground of VMODEM Vout
G15, G16	GND_VMODEM	GND	VMODEM ground
C15	GND_VGPU_FB	I	Remote sense on ground of VGPU Vout
D12, D13	GND_VGPU	GND	VGPU ground
E12	GND_VDRAM1_FB	I	Remote sense on ground of VDRAM1 Vout
H15	GND_VDRAM1	GND	VDRAM1 ground
B16	GND_VCORE_FB	I	Remote sense on ground of VCORE
A13, B13	GND_VCORE	GND	VCORE ground
E1	GND_SMPS	GND	GND of buck controller
L6	FSOURCE	PWR	EFUSE power source
G2	FLYP	O	Flying capacitor top
F2	FLYN	O	Flying capacitor bottom
E5	EXT_PMIC_EN2	O	Ext chip enable pin2
D3	EXT_PMIC_EN1	O	Ext chip enable pin1
L8	DVSS18_IO	GND	Digital IO power GND
L9	DVDD18_IO	PWR	Digital IO power
J8	DVDD18_DIG	PWR	VDIG18 output voltage
F7, F8, F9, G7, G8, G9, H7, H8, H9	D_GND	GND	Ground
N6	CS_P	I	Fuel gauge ADC input pin
M5	CS_N	I	Fuel gauge ADC input pin
K13	CHRLDO	O	CHRLDO output voltage
L12	BATON	I	Battery NTC pin for battery and its temperature sensing
L13	BATADC	I	Fuel gauge ADC input pin for monitoring battery voltage

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Ball	Symbol	I/O	Description
J5	AVSS28_AUD	GND	Audio UL ground
R2	AVSS22_XOBUF	GND	Ground for XO
N2	AVSS22_XO_ISO	GND	Connect to GSUB for DCXO noise isolation
P2	AVSS22_XO	GND	Ground for XO
M4	AVSS18_AUXADC	GND	AUXADC ground
H1	AVSS18_AUD	GND	Audio DL ground
J3	AVDD28_AUD	PWR	Power supply of Audio UL
M3	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
H2	AVDD18_AUD	PWR	1.8V power supply of audio
M2	AUXADC_VIN	I	AUXADC input
K10	AUD_SYNC_MOSI	I/O	Audio control interface
J10	AUD_SYNC_MISO	I/O	Audio control interface
L10	AUD_DAT_MOSI1	I/O	Audio control interface
J9	AUD_DAT_MOSI0	I/O	Audio control interface
H11	AUD_DAT_MISO1	I/O	Audio control interface
J11	AUD_DAT_MISO0	I/O	Audio control interface
L11	AUD_CLK_MOSI	I	Audio control interface
H10	AUD_CLK_MISO	O	Audio control interface
K4	AU_VIN2_P	I	Microphone channel 2 positive input
K3	AU_VIN2_N	I	Microphone channel 2 negative input
L4	AU_VIN1_P	I	Microphone channel 1 positive input
L3	AU_VIN1_N	I	Microphone channel 1 negative input
K1	AU_VIN0_P	I	Microphone channel 0 positive input
L1	AU_VIN0_N	I	Microphone channel 0 negative input
F1	AU_V18N	PWR	Audio -1.8V supply
H5	AU_REFN	GND	Audio reference ground
L5	AU_MICBIAS1	O	Microphone Bias 1
K5	AU_MICBIAS0	O	Microphone Bias 0
G5	AU_LOLP	O	Lineout positive output
G6	AU_LOLN	O	Lineout negative output

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Ball	Symbol	I/O	Description
J6	AU_HSP	O	Handset positive output
H6	AU_HSN	O	Handset negative output
G4	AU_HPR	O	Earphone right channel output
H4	AU_HPL	O	Earphone left channel output
K6	ACCDET	I	Accessory detection input

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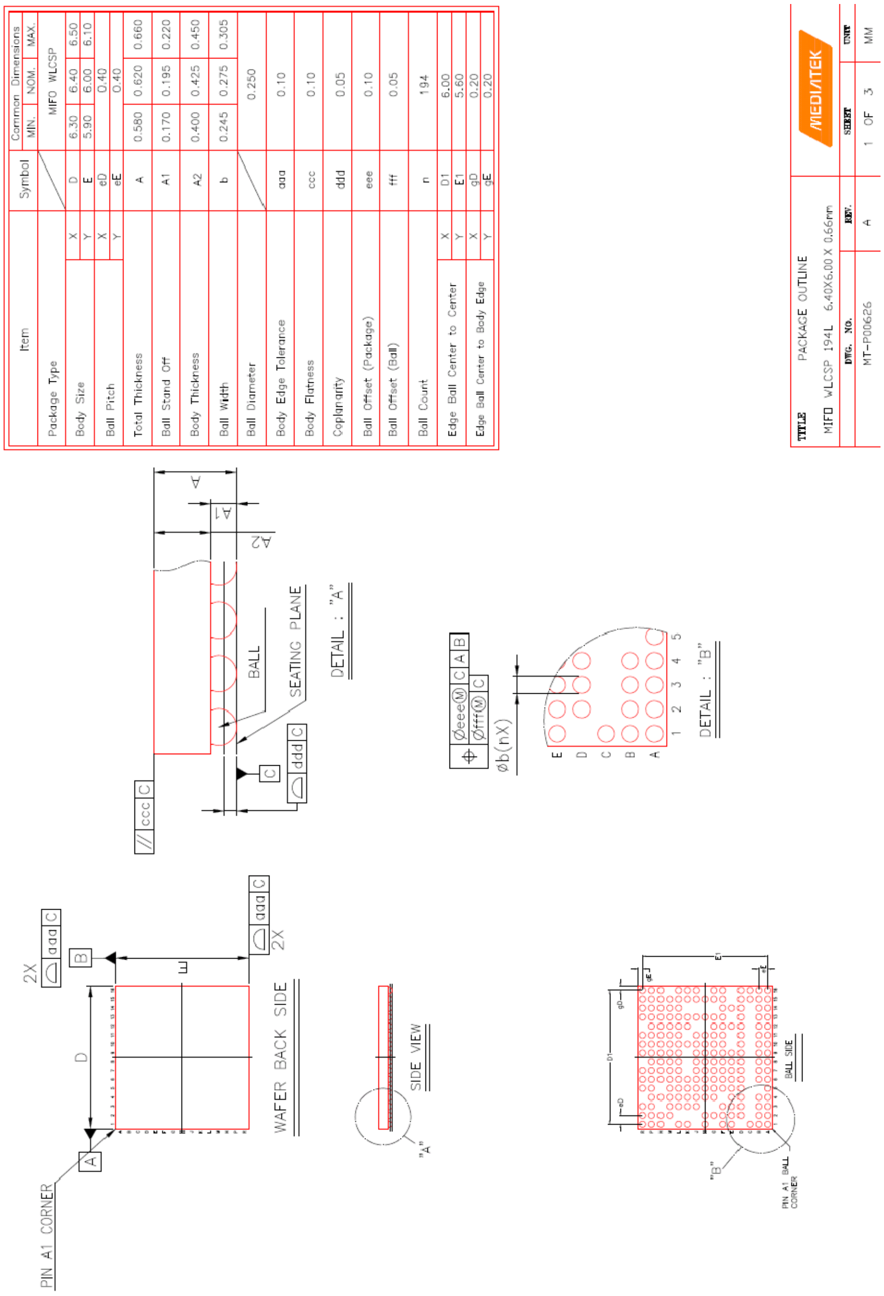
2 MT6358 Packaging

2.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				MIFO WLCSP	
Body Size	X	D	6.30	6.40	6.50
	Y	E	5.90	6.00	6.10
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Total Thickness		A	0.580	0.620	0.660
Ball Stand Off		A1	0.170	0.195	0.220
Body Thickness		A2	0.400	0.425	0.450
Ball Width		b	0.245	0.275	0.305
Ball Diameter				0.250	
Body Edge Tolerance		aaa		0.10	
Body Flatness		ccc		0.10	
Coplanarity		ddd		0.05	
Ball Offset (Package)		eee		0.10	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		194	
Edge Ball Center to Center	X	D1		6.00	
	Y	E1		5.60	
Edge Ball Center to Body Edge	X	gD		0.20	
	Y	gE		0.20	

Figure 2-1. Package dimension

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Appendix

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